CVC: Circuit Validity Check

Overview:

Some IC design errors are not readily detectable with standard front-end SPICE and Verilog simulation or back-end LVS and DRC verification. These errors include leaks due to intermittent floating inputs or shorts, problems with signals crossing differing voltage domains, errors related to input and output of cutoff regions, and errors due to integrating varying IP. CVC is designed to pinpoint these types of errors and is able to verify a full design quickly. Similar tools include: Synopsys' CustomSim Circuit Check(CCK), Mentor Graphics' Calibre PERC, Cadence's PVS PERC.

Merits:

Fast: 70M gate design read in 5 minutes, total run time 45 minutes. (Linux RedHatE5, Intel Xeon E5-2690, 256GB).
High capacity: 100M+ gate designs can be checked.
Comprehensive: All error types detected in single execution.
Error management: Errors are marked with references and classified by severity. Fewer missed errors. Easier review.

Input:

- CDL netlist used for Calibre LVS (full chip simulation is recommended).
- Power settings (Excel):
  Nets are defined as power (fixed voltage), input (minimum and/or maximum and/or simulation level), or internal nets. Power may be defined as "open".
- Device settings(Excel):
  Basic devices are mosfet, resistors, capacitors , diodes and bipolar transistors. These devices may be defined as switches (on/off) or fuses (on/off).

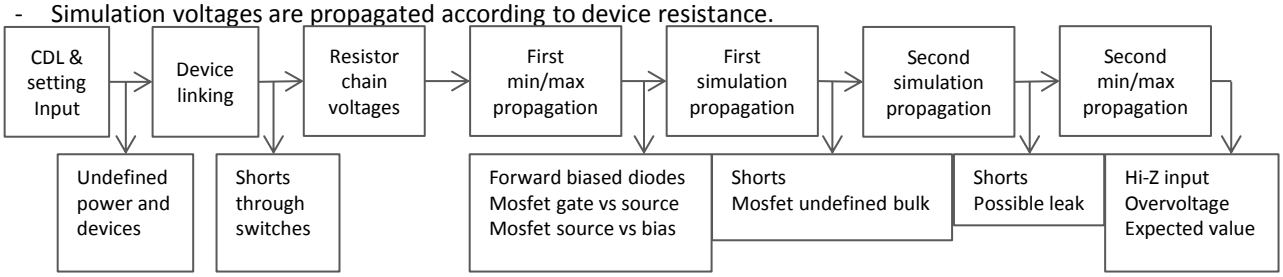
Output:

- Individual device error list with connected nets.
- Error summary list with error counts by error type.

Algorithm:

CVC performs 3 types of voltage propagation using event queues.

- Minimum voltages and maximum voltage propagations are performed concurrently. The minimum voltage propagation is from the least voltage to the greatest voltage, while maximum voltage propagation is from the greatest voltage to the least voltage. Maximum voltage propagation includes Vth drops through N-type mosfets and is limited by maximum gate voltage. Minimum voltage propagation include Vth step-ups through P-type mosfets and is limited by minimum gate voltage. Depletion mosfet are also handled. Mosfet connected as diodes result in Vth drop if there are no other connections.
- Simulation voltages are propagated according to device resistance.



- The first min/max propagation includes mosfets that are in cutoff mode while the second min/max propagation does not. The second min/max propagation is used to determine leak paths.
- The first sim propagation is for fixed power only and is used to detect mosfet undefined bulk connections.

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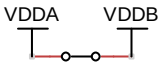
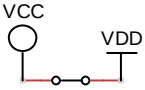
Error types:

- Undefined power and devices: all power definitions must exist in netlist and all device models must be defined in the device file. Device definitions may be differentiated by parameters (e.g. L>100nm).
- Shorts through switches: Different metal masks may be created by using metal switches (resistors or capacitors in the netlist). For normal simulation, a different netlist is required for each mask. However, both mask configurations can be verified with one netlist using CVC by changing the switch definitions in the device file. Nets shorted via switches are considered to be the same net.

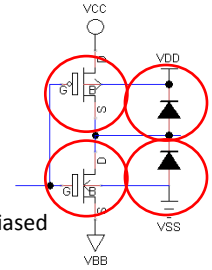


Warning for same voltages



Error for different voltages

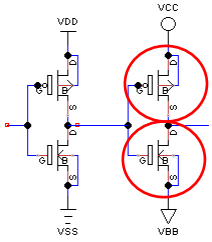
- Forward bias diodes
  including mosfet bulk-source/drain diodes



VCC > VDD
PMOS source-bulk is forward biased
Output ESD (VDD) diode may be forward biased

VBB < VSS
NMOS bulk-source is forward biased
Output ESD (VSS) diode may be forward biased

- Mosfet gate vs source: mosfets that are always on because the max gate voltage < max source voltage for pmos, or the min gate voltage > min source voltage for nmos.

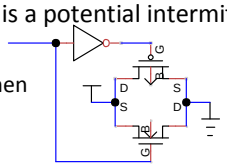


VDD < VCC
PMOS is always on

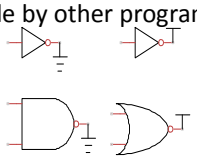
VSS > VBB
NMOS is always on

- Shorts: all shorts between power signals are reported and other shorts (input, internal nets) are reported if the current exceeds a specified limit.
- Mosfet undefined bulk: generally, this indicates a missing power definition.
- Possible leak: Mosfet error where the source and drain are connected to different power nets and the gate level is indeterminate. This is a potential intermittent error that is not readily detectible by other programs.

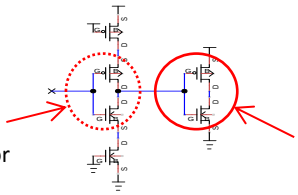
Short only when input is high



Also detects these errors



- Hi-Z input: logically undriven gates.



Hi-Z input but no leak path therefore no error

Hi-Z input with leak path therefore error

- Overvoltage: detected if the maximum voltage difference exceeds the specified tolerance for each device/terminal combination. For mosfets, the gate-source, source-drain, source-bulk, gate-bulk checks are all possible.
- Expected values: expected values can be set for minimum, maximum, and simulation voltages. An error is generated if the calculated value does not match the expected value. It is possible to expect undriven (open) nets.

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License:

- CVC is released under the open-source GPLv3 license.

ShuhariSystem Support:

- Maintenance contract: There are no guarantees for software released under GPLv3. However, ShuhariSystem provides a time-based maintenance contract that covers installation support and bug fixes. Other training and requests for additional checks will be handled separately on a case-by-case basis.

- Third-party verification: As with other verification tools, the settings to detect the desired errors with minimal false errors require some degree of experience. To decrease designers' burden of learning a new tool, ShushariSystems offers an on-site third party verification service on a per chip basis.
  The cost is based on the number of gates/memory size, the number of modes, and the number of requests.

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